Exercise 1. [10 points] The following statements are either [T]rue or [F]alse. Indicate T in [ ] if the statement is true, otherwise F in [ ].

1.1 [F] There is a one-to-one correspondence between truth table and gate diagram directly.

1.2 [F] Multiplexors are state elements.

1.3 [T] A multiplexor is used to select from among several inputs based on the setting of its control lines.

1.4 [T] In a single-cycle datapath, the fourth stage, Memory Access, that we studied in class is designed for load and store instructions only.

1.5 [F] Each MIPS instruction always takes full use of five stages of the datapath.

1.6 [T] Register file behaves as a combinational logic block during the read operation.

1.7 [T] The longest path through the datapath determines the length of clock period for a single-clock CPU.

1.8 [F] For a single-clock CPU, register or memory write stage of an instruction finishes in the same clock cycle as this instruction does instruction fetch and decode.

1.9 [F] To support 6 types of arithmetic operations in the ALU, one shall use at least 4 bits of control lines.

1.10 [F] Control unit is controlled by the datapath to perform operations.
Exercise 2. [20 points] Consider the following MIPS instruction.

\[ \text{slti } rt, rs, 17 \]  # if (Reg[rs] < 17) Reg[rt] = 1
# else Reg[rt] = 0

Figure 1 shows a simple implementation of the datapath for 5 stages.

Figure 1: Generic Steps of Datapath

2.1 Describe what each stage of the datapath does for this instruction.

Stage 1: fetch this instruction [1], increment PC [1]

Stage 2: decode to determine it is an slti [1], then read register rs [1]

Stage 3: compare value retrieved in Stage 2 with the integer 17 [2]
Stage 4: idle [2]

Stage 5: write the result of Stage 3 (1 if $rs < 17$, 0 otherwise) into register $rt$ [2]

2.2 Indicate the wires from (1) - (14), such that the wire has the needed value for executing this $slti$ instruction.

(1) - (4) (7) (8) (9) (10) (13) (14) [1] for each
Exercise 3.  [20 points] You are given a single cycle datapath with control signals in Figure 2.

Figure 2: A Single Cycle Datapath

3.1 For the instruction `slti` in Exercise 2, give the value of each of the 8 control signals.

<table>
<thead>
<tr>
<th>Control Signal</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>nPC_sel</td>
<td>0 or ‘+4’ [2]</td>
</tr>
<tr>
<td>RegDst</td>
<td>0 or ‘Rt’ [2]</td>
</tr>
<tr>
<td>RegWr</td>
<td>1 [2]</td>
</tr>
<tr>
<td>ExtOp</td>
<td>1 or ‘signed’ [2]</td>
</tr>
<tr>
<td>ALUsrc</td>
<td>1 or ‘imm’ [2]</td>
</tr>
<tr>
<td>ALUctr</td>
<td>‘&lt;’ [2]</td>
</tr>
<tr>
<td>MemWr</td>
<td>0 [2]</td>
</tr>
<tr>
<td>MemtoReg</td>
<td>0 or ‘ALU’ [2]</td>
</tr>
</tbody>
</table>


3.2 At which stage (1 - 5), those control signals are computed and sent to the datapath?

Stage 2 decode. [2]

3.3 When is PC updated to store the next instruction address? Note that PC is a register that is triggered by the rising edge of clock for the write operation.

PC is updated at stage 1 instruction fetch [1], but since PC is a register, the value will be written to PC on the rising edge of the next clock cycle. [1]